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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,672	06/18/2001	Takeshi Kuribayashi	2001_0771	7635

513 7590 05/26/2005

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,672	KURIBAYASHI ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-33, 35, 36 and 48-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-33, 35, 36 and 48-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26, 30, 31, 32, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,512,712 (hereafter Iwata).

Examiner notes the limitation "wherein said at least one recognition mark is formed on said surface simultaneously with formation of said lands on said electrical connecting surface" is a process limitation in a device claimed and is thus only considered to the extent to which said process impacts the structure of the device. Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Iwata discloses, referring to figures 1 & 2, an electronic component (10) to be mounted on a printed board, said electronic component comprising; an electrical connecting surface; a plurality of lands (20b) provided on said electrical connecting surface in arrangement positions within a contour of said electronic component; and at least one recognition mark (40, 20a) located on a surface of the electronic component

and serving as a reference for the arrangement positions of said electrical connecting portions (see col. 3, lines 20-25)[claim 26]. Regarding the limitation that the device is "to be mounted on a printed board", this limitation has been considered only to the extent that any alleged prior art must be capable of performing this intended use. In the instant rejection, it is the Examiner's position that the device of Iwata could indeed be mounted on a printed such as in a motherboard – daughterboard combination as is common in the art. Since there is no structural difference between the claimed invention and the device of Iwata and the device of Iwata is capable of being mounted on a printed board, the claimed invention is anticipated.

Furthermore, Iwata discloses wherein said recognition mark comprises a projection or a printed symbol [claim 30], wherein said recognition mark includes coded information indicative of said electronic component (see col. 3, lines 10-15) [claim 31], wherein the coded information of said recognition mark is information concerned with a state in which the electrical connecting portions are formed [claim 32], wherein said electrical connecting portions (20b) are lands [claim 36].

Claims 26-30, 35, 49-55, 57 and 58 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,726,502 (hereafter Beddingfield).

Examiner notes the limitation "wherein said at least one recognition mark is formed on said surface simultaneously with formation of said lands on said electrical connecting surface" is a process limitation in a device claimed and is thus only considered to the extent to which said process impacts the structure of the device.

Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Beddingfield discloses, referring to figures 2-5, an electronic component (32) to be mounted on a printed board (34), said electronic component comprising; an electrical connecting surface; a plurality of lands (42, 52, 62, 72) provided on said electrical connecting surface in arrangement positions within a contour of said electronic component; and at least one recognition mark (38, 54, 64, 74) located on a surface of the electronic component and serving as a reference for the arrangement positions of said electrical connecting portions (see col. 4, lines 20-45) [claim 26], wherein said at least one recognition mark comprises a pair of recognition marks (54) positioned symmetrically with respect to a center point of said electrical connecting surface, wherein said electrical connecting portions (52) are disposed in an array that surrounds said recognition marks, wherein said at least one recognition mark comprises a plurality of recognition marks (54) that are positioned symmetrically with respect to a center point of said electrical connecting surface [claim 27], wherein said recognition marks are located in a central portion of said electrical connecting surface, and said electrical connecting portions are disposed around said recognition marks [claim 28], wherein said recognition mark is provided on a side of said electrical connecting surface that is adapted to confront a mounting position of the printed board [claim 29], wherein said recognition mark comprises a projection or a printed symbol [claim 30], wherein said electrical connecting portions are solder bumps (see col. 4, lines 10-20) [claim 35];

wherein said surface is said electrical connecting surface [claims 49, 57], further comprising a solder bump (36) on each of said lands [claim 51], wherein said at least one recognition mark comprises a pair of recognition marks positioned symmetrically with respect to a center point of said electrical connecting surface, wherein said lands are disposed in an array that surrounds said pair of recognition marks (see figure 2) [claim 52], wherein said at least one recognition mark comprises plural recognition marks that are positioned symmetrically with respect to a center point of said electrical connecting surface, wherein said plural recognition marks are located in a central portion of said electrical connecting surface, and said lands are disposed around said plural recognition marks (see figure 2) [claim 53], wherein said at least one recognition mark is provided on a side of said electrical connecting surface that is adapted to confront a mounting position of the printed board [claim 54], wherein said at least one recognition mark comprises a projection or a printed symbol [claim 55].

Regarding claims 50 and 58, the limitation "wherein said at least one recognition mark and said lands are formed simultaneously on said electrical connecting surface by using a mask" is a process limitation in a device claimed and is thus only considered to the extent to which said process impacts the structure of the device. Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Claims 26, 30, 33, 48, 51, and 56 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,805,421 (hereafter Livengood).

Examiner notes the limitation "wherein said at least one recognition mark is formed on said surface simultaneously with formation of said lands on said electrical connecting surface" is a process limitation in a device claimed and is thus only considered to the extent to which said process impacts the structure of the device. Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Livengood discloses, referring to figures 3a-3e, an electronic component (40) to be mounted on a printed board (43), said electronic component comprising; an electrical connecting surface; a plurality of lands (bond pads referred to, but not shown, see col. 5, lines 5-20) provided on said electrical connecting surface in arrangement positions within a contour of said electronic component; and at least one recognition mark (34, 35) located on a surface of the electronic component and serving as a reference for the arrangement positions of said electrical connecting portions (see col. 3, lines 20-30) [claim 26], wherein said recognition mark comprises a projection or a printed symbol [claim 30], wherein said recognition mark is located in a corner portion of an opposite side of the electronic component relative to said electrical connecting portion (see figure 3d) [claim 33], further comprising a solder bump (42) on each of said lands [claim 51], wherein the recognition mark does not project from the surface of the electronic component [claims 48, 56].

Response to Arguments

Applicant's arguments filed 18 February 2005 have been fully considered but they are not persuasive. Regarding Iwata, Applicants argue that Iwata "fails to teach or suggest an electronic component" since the invention of Iwata is specifically characterized as a printed circuit board. However, it is well understood by the ordinarily skilled artisan that a PCB is indeed an electronic component that may be further mounted on another circuit board in a motherboard-daughter board relationship. With regard to Beddingfield, Applicants proffer "Beddingfield fails to teach or suggest that alignment bumps 38 are formed simultaneously with pads or lands 39". However, as stated above, this limitation is a process limitation in a device claimed and is thus only considered to the extent to which said process impacts the structure of the device. Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)). Similarly, regarding Livengood Applicants' allege that the limitation "that the at least one recognition mark is formed simultaneously with the lands" distinguishes the claimed invention from the prior art. However, as stated above, this limitation is a process limitation in a device claimed and is thus only considered to the extent to which said process impacts the structure of the device. Moreover, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Having addressed each of Applicants' arguments, the traversal of the rejection on these grounds is deemed unsuccessful.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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